1. A single transistor ferroelectric memory cell, comprising:

a semiconductor substrate having defined thereon:

a first conductive region of a first conductive type;

a source region of a second conductive type defined in said first conductive region, said source region sized and configured to comprise a portion of the ferroelectric memory cell and an adjacent ferroelectric memory cell; and

a drain region also of a second conductive type defined in said first conductive region, said drain region being spaced apart from said source region such that a channel region comprising a portion of said first conductive region is defined between said source region and said drain region;

a gate oxide layer disposed on said semiconductor substrate to cover said drain, channel, and source regions;

a ferroelectric gate unit disposed on said gate oxide layer comprising:

a bottom electrode in electrical communication with said drain region;

a top electrode;

a ferroelectric layer disposed between said bottom and said top electrode; and

a sealing layer disposed on each side of said ferroelectric gate unit; and

an upper conductive layer disposed on said ferroelectric gate unit and a portion of said gate oxide coating such that said upper conductive layer and said top electrode of said ferroelectric gate unit are in electrical communication.

2. A single transistor ferroelectric memory cell as defined in claim 1, wherein said upper conductive layer comprises polysilicon doped to a conductive state.

3. A single transistor ferroelectric memory cell as defined in claim 1, further comprising a plurality of shallow isolation trenches defined in the semiconductor substrate.

4. A single transistor ferroelectric memory cell as defined in claim 1, further comprising a lower polysilicon layer disposed between said gate oxide layer and said bottom electrode, the lower polysilicon layer doped to a conductive state and having a thickness a thickness of from about 500 to 700 Å.

5. A single transistor ferroelectric memory cell as defined in claim 1, wherein said first conductive region of a first conductive type includes ions implanted therein, said ions taken from the group consisting of B and BF_2.

6. A single transistor ferroelectric memory cell as defined in claim 1, wherein said source and drain regions of a second conductive type include ions implanted therein, said ions taken from the group consisting of P and As.

7. A single transistor ferroelectric memory cell as defined in claim 1, wherein said bottom and top electrode are composed of material taken from the group consisting of Pt, Ir, IrO_2, Ru, and RuO, said bottom and top electrode each having a thickness of about 500 to 1,500 Å.

8. A single transistor ferroelectric memory cell as defined in claim 1, wherein said ferroelectric layer is comprised of material taken from the group consisting of Pb(Zr, Ti)O_3, $SrBiTa_2O_9$, $Pb_5Ge_3O_{11}$, and $BaTiO_3$, said ferroelectric layer having a thickness of about 800 to 2,000 Å.

9. A single transistor ferroelectric memory cell as defined in claim 1, wherein said sealing layer comprises material taken from the group consisting of Si_3N_4 and Al_2O_3.

10. A single transistor ferroelectric memory cell as defined in claim 1, wherein the spacing between said source region and said drain region is approximately .18 to .35 μm.

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11. A method for forming a single transistor ferroelectric memory cell, the method comprising the steps of:

providing a semiconductor substrate;

implanting ions in said semiconductor substrate to form a first conductive region of a first conductive type;

implanting ions in said first conductive region to form a source region of a second conductive type and a drain region also of a second conductive type, said source region being spaced apart from said drain region such that a channel portion of said first conductive region resides between said source region and said drain region, said source region also disposed such that it comprises a portion of the present ferroelectric memory cell and a portion of an adjacent ferroelectric memory cell;

disposing on said channel region, drain region, and at least a portion of said source region a gate oxide layer;

disposing on said gate oxide layer a ferroelectric gate unit such that said drain region, said channel region, and at least a portion of said source region are covered thereby, the ferroelectric gate unit comprising:

a bottom electrode, said bottom electrode sized and configured to be in electrical communication with said drain region, the drain region also comprising the bit line for the memory cell;

a ferroelectric layer; and

a top electrode;

coating said ferroelectric gate unit and at least a portion of said source region with an upper polysilicon layer such that said top electrode of said

ferroelectric gate unit is in electrical communication with said upper polysilicon layer; and

doping said upper polysilicon layer to a conductive state.

12. A method for forming a single transistor ferroelectric memory cell as defined in claim 11, further comprising the step of

forming on the structure resulting from the previous step a source electrode, a drain electrode and an upper polysilicon layer electrode.

13. A method for forming a single transistor ferroelectric memory cell as defined in claim 12, further comprising the step of:

forming a lower polysilicon layer over said gate oxide layer and beneath said ferroelectric gate unit, the lower polysilicon layer having a thickness of from about 500 to 700 Å;

14. A method for forming a single transistor ferroelectric memory cell as defined in claim 13, further comprising the step of:

doping said lower polysilicon layer to a conductive state.

15. A method for forming a single transistor ferroelectric memory cell as defined in claim 14, further comprising the step of:

isolating the ferroelectric memory cell by defining shallow trenches in the semiconductor substrate.

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16. A method for forming a single transistor ferroelectric memory cell as defined in claim 15, further comprising the step of:

depositing a sealing layer on each side of said ferroelectric gate unit, said sealing layer comprising material taken from the group consisting of Si_3N_4 and Al_2O_3.

17. A method for forming a single transistor ferroelectric memory cell as defined in claim 16, wherein the gate oxide layer comprises SiO_2.

18. A method for forming a single transistor ferroelectric memory cell as defined in claim 17, wherein the implanting ions in said semiconductor substrate to form a first conductive region step includes implanting a dopant for taken from the group consisting of B or BF_2.

19. A method for forming a single transistor ferroelectric memory cell as defined in claim 18, wherein the implanting ions in said first conductive region step includes implanting a dopant for source and drain regions of second conductive type taken from the group consisting of P and As.

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20. A method for forming a single transistor ferroelectric memory cell as defined in claim 19, wherein said bottom and top electrode are composed of material taken from the group consisting of Pt, Ir, IrO_2, Ru, and RuO, said bottom and top electrode each having a thickness of about 500 to 1,500 Å.

21. A method for forming a single transistor ferroelectric memory cell as defined in claim 20, wherein said ferroelectric layer is comprised of material taken from the group consisting of $Pb(Zr, Ti)O_3$, $SrBiTa_2O_9$, $Pb_5Ge_3O_{11}$, and $BaTiO_3$, said ferroelectric layer having a thickness of about 800 to 2,000 Å.

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22. A ferroelectric memory cell comprising:

a ferroelectric gate unit comprising a top electrode, a layer of ferroelectric material, and a bottom electrode;

a semiconductor substrate having:

a drain;

a source;

a channel;

a gate oxide; and

means for controlling the polarization of said layer of ferroelectric material.

23. A ferroelectric memory cell as defined in claim 22, wherein the means for controlling the polarization of said layer of ferroelectric material comprises an electrical connection between said drain and said bottom electrode of said ferroelectric gate unit.

24. A ferroelectric memory cell as defined in claim 23, wherein the means for controlling the polarization of said layer of ferroelectric material further comprises an upper polysilicon layer deposited on top of said ferroelectric gate unit such that electrical communication is established between said top electrode and said conducting polysilicon layer.

25. A ferroelectric memory cell as defined in claim 22, further comprising a lower polysilicon layer deposited between the ferroelectric gate unit and the gate oxide.

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26. A method for programming a ferroelectric memory cell having a ferroelectric gate unit comprising a top electrode, a ferroelectric layer, and a bottom electrode, the memory cell also having a semiconductor substrate comprising a source region and drain region of a first conductive type, the source region configured to comprise a portion of the present ferroelectric memory cell and an adjacent ferroelectric memory cell, and a channel between said source region and drain region of a second conductive type, a gate oxide layer being disposed between said semiconductor substrate and said ferroelectric gate unit, and a conductive top layer disposed on said ferroelectric gate unit and at least a portion of said source region, the method comprising the steps of:

applying a positive voltage to the drain region, thereby charging the bottom electrode of the ferroelectric gate unit; and

grounding the conductive top layer, thereby grounding the top electrode of the ferroelectric gate unit and polarizing the ferroelectric layer of the ferroelectric gate unit to a programmed polarization.

27. A method for programming a ferroelectric memory cell as defined in claim 26, wherein the positive voltage applied to the drain region is in the range of about 3 to 8 V.

28. A method for erasing a ferroelectric memory cell having a ferroelectric gate unit comprising a top electrode, a ferroelectric layer, and a bottom electrode, the memory cell also having a semiconductor substrate comprising a source region and drain region of a first conductive type, the source region configured to comprise a portion of the present ferroelectric memory cell and an adjacent ferroelectric memory cell, and a channel between said source region and drain region of a second conductive type, a gate oxide layer being disposed between said semiconductor substrate and said ferroelectric gate unit, and a conductive top layer disposed on said ferroelectric gate unit and at least a portion of said source region, the method comprising the steps of:

applying a positive voltage to the conductive top layer, thereby charging the top electrode of the ferroelectric gate unit; and

grounding the drain region such that the ferroelectric layer of the ferroelectric gate unit is polarized to an erased polarization.

29. A method for programming a ferroelectric memory cell as defined in claim 28, wherein the positive voltage applied to the conductive layer is in the range of about 3 to 8 V.

30. A method for reading a ferroelectric memory cell having a ferroelectric gate unit comprising a top electrode, a ferroelectric layer, and a bottom electrode, the memory cell also having a semiconductor substrate comprising a source region and drain region of a first conductive type, the source region configured to comprise a portion of the present ferroelectric memory cell and an adjacent ferroelectric memory cell, and a channel between said source region and drain region of a second conductive type, a gate oxide layer being disposed between said semiconductor substrate and said ferroelectric gate unit, and a conductive top layer disposed on said ferroelectric gate unit and at least a portion of said source region, the method comprising the steps of:

applying a positive voltage to the conductive top layer;

applying a positive voltage to the drain region;

grounding the source region; and

providing sensing circuitry electrically connected to the ferroelectric memory cell to enable reading of the resulting level of current passing through the channel region.

31. A method for programming a ferroelectric memory cell as defined in claim 30, wherein the positive voltage applied to the conductive top layer and the drain region is in the range of about 3 to 8 V.